

CH 08 LOGIC FAMILIES

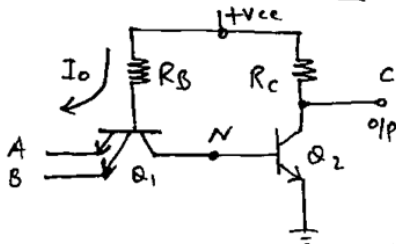
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LOGIC Families 8-

TYPES 8- There following types of Logic families.

- ① DTL ② RTL ③ TTL ④ Schottkey TTL ⑤ MOSFET ⑥ CMOS
 * DTL & RTL are discussed in previous chapter #02

Basic circuit of TTL 8- Basic set of TTL is NAND Gates-



Working: ① Q1 is double emitter transistor are used

② When A & B = 0 then current I_0 flow through twice emitter and point "N" will be at "0" logic

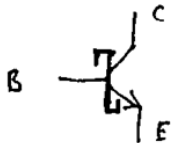
So Q2 will be off & output $C = 1$

③ A=0, B=1 OR A=1, B=0 :- is same as above but now I_0 flow through that emitter which's input is zero. $N=0$ $C=1$

④ A=1 & B=1 Now Base to emitter junction of Q1 will be reverse bias & Base to collector junction will be forward. point $N=1$ Q2 = ON and off $C=0$.

Schottkey TTL Just Replace the TTL transistor by schottkey transistor, its use for high Speed Switching.

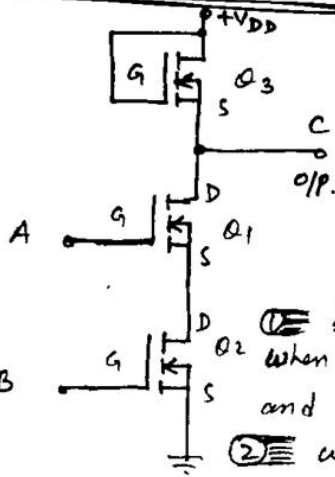
Schottkey transistor



MOSFET :- there are Basically two types of MOSFET ① N channel & ② P-channel.

here we will discuss only n-channel & only Universal Gates at.

NMOS NAND Gate:-



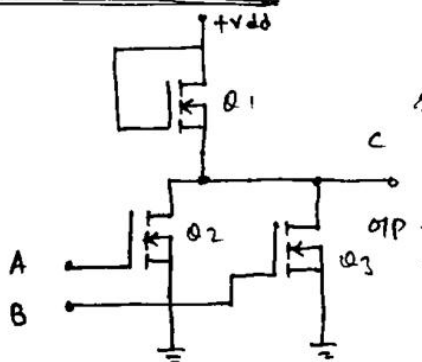
Working:-

① When $A \& B = 1$ then $Q_1 \& Q_2$ will be ON and V_{DD} will drop across Q_3 & o/p $C = 0$

② When any input A or B or twice $A \& B = 0$ then that "0" transistor (MOSFET) will OFF

& o/p $C = 1$.

NMOS NOR Gate



Working:-

① When $A \& B = 0$ the o/p $C = 1$

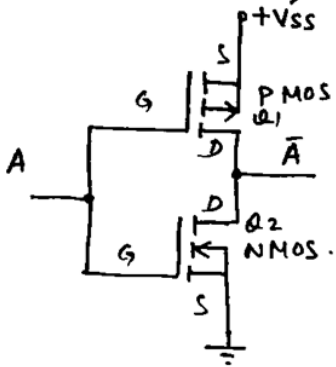
② When any input or twice $A \& B = 1$ then that "0" will be ON & current pass through Q_1 & that ORN transistor

$+V_{DD}$ drop across Q_1 & o/p $C = 0$

* Other Gates Draw your self by using this technique & follow the RTL logic.

CMOS → Complementary metal oxide Semiconductor FET
 Basically in CMOS two MOSFET are used N-MOS & P-MOS
 So it's called CMOS.

Basic cell:-



Basic cell of CMOS is NOT Gate.

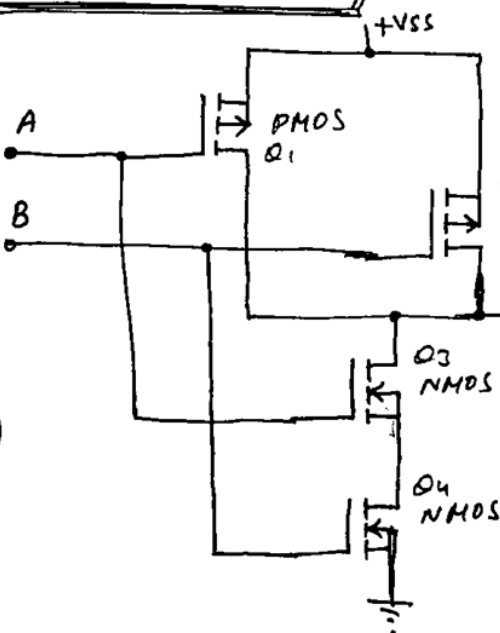
- ① Gate Short will Gate
 - ② Drain with Drain
 - ③ +Vss at PMOS Source & NMOS Source is Grounded
- input at Gate & output through Drain.

Working:-

$A = 1$, $Q_1 = \text{OFF}$ & $Q_2 = \text{ON}$, So no current flow & out-
 $\bar{A} = 0$

$A = 0$, $Q_1 = \text{ON}$ & $Q_2 = \text{OFF}$, So current flow toward o/p
 $\bar{A} = 1$.

CMOS NAND Gate



Working:-

① $A, B = 0$, $Q_1, Q_2 = \text{ON}$, $Q_3, Q_4 = \text{OFF}$
 current flow through Q_1 & Q_2
 toward o/p $C = 1$

② any one "0" same
 condition.

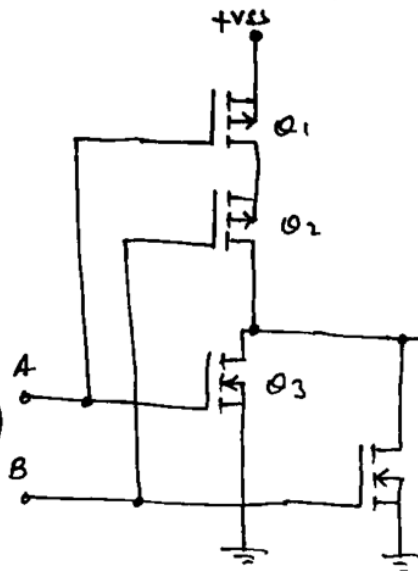
③ $A = 1$ $B = 1$

Q_1 & $Q_2 = \text{OFF}$, $Q_3, Q_4 = \text{ON}$
 No current flow so o/p $C = 0$

CMOS NOR Gate

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Working:-



$$A \text{ \& } B = 0$$

$Q_1 \text{ \& } Q_2 \text{ ON \& } Q_3 \text{ \& } Q_4 = \text{OFF}$

current flow through $Q_1 \text{ \& } Q_2$
toward o/p $c = 1$

o/p Any one = 1 OR Twice $AB = 1$

$c =$ Relevant "0" from $Q_1 \text{ \& } Q_2$

will be OFF whichs input = 1

So no current flow through
circuit and out-put $c = 0$

* you will be Explain by heading of each i/p Separate in paper.

[Signature]
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